

## **CLAIMS**

1. A power oscillator for controlling the wave shape and amplitude of an input  
2 signal to produce a desired output signal, the circuit comprising:  
a tapped delay line connected to the input signal, the tapped delay line  
4 having a plurality of taps, each tap separated from an adjacent tap  
to produce a plurality of delayed input signals;  
6 at least one buffer, the buffer comprising:  
a plurality of input lines connected to the plurality of taps;  
8 an input voltage line for connection to a controllable voltage  
source; and  
10 a plurality of output lines; and  
a plurality of impedance elements having first ends connected to the  
12 plurality of output lines, the plurality of impedance elements having  
second ends connected in parallel to an output node to produce  
14 the desired output signal.
2. The power oscillator of claim 1, wherein the desired output signal is coupled  
2 to an antenna of a smart card through an impedance matching circuit.
3. The power oscillator of claim 1, wherein the plurality of impedance elements  
2 are one of reactive elements and lossy elements.
4. The power oscillator of claim 1, wherein each impedance element of the  
2 plurality of impedance elements comprises a reactive element and a lossy  
element.
5. The power oscillator of claim 1, where in the input signal is 100% amplitude  
2 (on/off) modulated.
6. The power oscillator of claim 1, wherein the tapped delay line comprises a  
2 stripline embedded in a circuit board.
7. The power oscillator of claim 1, wherein the controllable voltage source limits  
2 the operating voltage of the buffer to produce an amplitude modulation less than  
100%.

- 2 8. A method for shaping and controlling the amplitude of an carrier signal, the  
method comprising the steps of:
- 4       inputting the carrier signal into a tapped delay line having a plurality of  
taps separated by a plurality of delay distances;
- 6       connecting each tap of the plurality of taps to a buffer of a plurality of  
buffers;
- 8       connecting an impedance element to an output of each buffer of the  
plurality of buffers;
- 10       connecting the outputs and impedance elements of each buffer in parallel  
to a single node to produce a shaped carrier signal; and
- 12       supplying a supply voltage to the buffers to control an output voltage  
amplitude of the shaped carrier signal.
9. The method of claim 8, wherein the plurality of delay distances are equal.
- 2 10. The method of claim 9, wherein the carrier signal is a square wave having  
a 50% duty cycle, and wherein the shaped carrier signal is trapezoidal.
- 2 11. The method of claim 8, further comprising the step of adding capacitive  
loading to the single node.
- 2 12. The method of claim 11, further comprising the step feeding the shaped  
carrier signal to an antenna tuned to the operating frequency of the carrier  
signal.
- 2 13. The method of claim 8, wherein the step of supplying a supply voltage to the  
buffers further comprises the steps of modulating the voltage of the power  
supply circuit resulting in a directly proportional modulation of the antenna field
- 4 in accordance with the desired percent modulation.
- 2 14. The method of claim 13, wherein the desired percent modulation is between  
0 and 25% modulation and the supply voltage is at a level of 5 volts.
- 2 15. The method of claim 14, wherein the desired percent modulation is between  
0 and 25% modulation and the supply voltage is at a level of 3.3 volts, using  
CMOS buffers operating at 3.3V.

2 16. The method of claim 8, wherein the plurality of delay distances are not equal, and the resulting shaped carrier signal is sinusoidal.

2 17. The method of claim 8, wherein the impedance element is one of a reactive element, a lossy element, and a combination of a reactive element and a lossy element.

2 18. A power oscillator for controlling the wave shape and amplitude of an input signal to produce a desired output signal, the circuit comprising:  
4 a tapped delay line means connected to the input signal, the tapped delay line means having a plurality of taps, each tap separated from an adjacent tap to produce a plurality of delayed input signals;  
6 at least one buffer means, the buffer means comprising:  
8 a plurality of input lines connected to the plurality of taps;  
an input voltage line for connection to a controllable voltage  
10 source; and  
a plurality of output lines; and  
12 a plurality of same-type impedance elements having first ends connected to the plurality of output lines, the plurality of same-type  
14 impedance elements having second ends connected in parallel to an output node to produce the desired output signal.

2 19. The power oscillator of claim 18, wherein the same-type impedance elements are one of resistive elements, inductive elements, and a combination of resistive elements and inductive elements.

2 20. The power oscillator of claim 18, wherein the desired output signal is coupled to an antenna of a smart card through an impedance matching circuit.